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REMARKS

The applicant thanks the Examiner Giles for the prudential examination. With respect to the Examiner's rejection, it is believed that the new claims 19-27 have distinguished the claimed subject matters from the cited reference, Toyoda et al. (US Publication No. 2003/0063202).

As a brief summary, the Examiner has rejected claims 1-18 based on Toyoda for the reason that Toyoda, in its Fig. 6 and paragraphs 0045 through 0069, has disclosed two thresholds and relevant determinations to be made based on the two thresholds.

However, the key feature of the present invention is not the determinations based on the two thresholds, but to reduce the image data amount to be processed, so that the processing speed may be increased, and the required memory (buffer) size may be reduced to save cost. This is done through the steps of: one-dimensionally identifying suspected defects (peaks), storing one-bit information thereof so that multi-bit image data become one-bit data for each pixel, and checking whether each peak is a defect. By this approach, the required buffer size is greatly reduced.

More specifically, in Toyoda, in addition to the A/D converter 4, two line buffers (Fig. 1, 1H delay 5 and 6) are required. The line buffers store multi-bit image data for each pixel. They are required because, as seen from Fig. 6 and paragraphs 0045 through 0069, Toyoda two-dimensionally compares a pixel (such as pixel B in Fig. 6) with its neighboring pixels (not only A and C, but also D, E and F). To do so, there must be a line buffer storing the image data of the pixels a1, A, a2, B, a3, C, and a4, and another line buffer storing the image data of the pixels b1, c1, b2, c2, b3, c3, and b4, so that the data therein may be used to compare with the output from the A/D converter 4

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(which are the image data of the pixels a5-a8). Moreover, please note that every pixel is represented by a multi-bit image data, so the size of the line buffers 5 and 6 are considerably large. Furthermore, the defective pixel detector 8 has to do multi-bit comparison among multiple pixels. As one may imagine, the processing time and hardware cost required to implement Toyoda are much less than optimum.

To the contrary, in the present invention, only one very small size buffer is required (see, specification of the present invention, page 8, lines 6-9; lines 14-22). Referring to Fig. 2 of the present invention, when a peak checking is made on the pixel (5, 6) (wherein 5 is the vertical coordinate and 6 is the horizontal coordinate), there is no need to store full multi-bit image data for every pixel in the previous row [(4, 2) to (5, 1)]. Instead, in the present invention, the line buffer 63 only stores a 1-bit indicator for each pixel in the previous row (see, specification of the present invention, page 8, lines 3-6). In other words, when a pixel [such as any of the pixels (4, 2) to (4, D)] is no more used for peak identification of another pixel (5, 6), but is still in a window for defect identification of that other pixel (5, 6), it is only required to store an indicator of the pixel [pixels (4, 2) to (4, D)]. Furthermore, this is also true when the window includes more than two rows; all the pixels that are no more used for peak identification, but may still be within a window for defect identification, can each be represented by a 1-bit indicator.

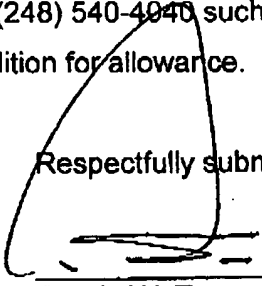
In view of the above, clearly the present invention may process image data with a much faster speed than Toyoda, and the required buffer size is much smaller. It should also be emphasized that, although a pixel is identified as a peak by one-dimensional determination, a peak is confirmed to be a defect by two-dimensional determination. Therefore, the accuracy of defect detection is not sacrificed.

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The applicant has amended the claims to highlight the aforementioned distinguishing features. All the currently pending claims are believed allowable over Toyoda. Such favorable action by the Examiner is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicant's representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,



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